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CONFIRMATION NO. 7277

## FILING RECEIPT



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## Applicant(s)

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## Assignment For Published Patent Application

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## Domestic Priority data as claimed by applicant

Technology Center 2600

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Non-Publication Request: Yes

Early Publication Request: No

## Title

Direct synthesis clock generation circuits and methods

**Preliminary Class**

375

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Title 37, Code of Federal Regulations, 5.11 & 5.15**

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ATTORNEY DOCKET NO.  
1064-CA

PATENT



**DIRECT SYNTHESIS CLOCK GENERATION  
CIRCUITS AND METHODS**

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**FIELD OF INVENTION**

[0001] The present invention relates in general to mixed signal circuitry, and in particular to direct synthesis clock generation circuits and methods..

**BACKGROUND OF INVENTION**

[0002] Often high functionality digital processing devices include multiple processing engines operating in response to clock signals of different frequencies. In other words, the speed of the clocks mediating the operation of various circuit blocks and other on-chip operational units may differ, depending on the function being implemented. These various clocks typically should be synchronous, especially when correlated data, such as audio and video, are being processed.

[0003] Traditional PLL techniques allow for the generation of multiple clock frequencies with relatively simple relationships. However, these frequencies are often insufficient to support disparate processing operations. For example, while processing an audio – video data stream, the video is typically processed at a clock frequency substantially higher than that used to process the audio. Moreover, the audio and video clocks may or may not be rationally related. In other words, it may not be possible to easily generate accurate synchronous audio and video clocks by simply dividing-down or multiplying-up a master clock in a PLL or similar circuit.